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EXAMINER	
SEDIGHIAN, REZA	

ART UNIT	PAPER NUMBER
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,829	DECUSATIS ET AL.	
	Examiner	Art Unit	
	M. R. Sedighian	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-27* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 7, it is not clear what is meant by "... the array of optical switching elements directs the optical byte of data from the at least one first set of ports in parallel to the at least one second set of ports notwithstanding that the at least some bits of optical data have different wavelengths." What does it mean by notwithstanding that the at least some bits of optical data have different wavelengths.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 8, 10, 19, 21, and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Akashi et al. (US Patent Application Publication No: 2003/0185493 A1).

Regarding claims 1, 19, and 25, Akashi teaches an optical switch (page 1, paragraph 0001, page 5, paragraph 0065 and fig. 9), comprising: at least one first set of ports (input port

group A, fig. 9) for receiving in parallel an optical byte of data (page 3, paragraph 0033, byte of optical data or information can be transmitted through the optical switch array 51); multiple second sets of ports (output ports group A and output ports group B, fig. 9), each being capable of outputting in parallel the optical byte of data (page 3, paragraph 0033); and an array of optical switching elements (51_{11}, 51_{14}, 51_{41}, 51_{44}, fig. 9) disposed between the first set of ports (input port group A, fig. 9) and the multiple second sets of ports (output ports group A and B, fig. 9), wherein the array of optical switching elements (51_{11}, 51_{14}, 51_{41}, 51_{44}, fig. 9) direct the optical byte of data in parallel from the first set of ports to one second set of ports of the multiple second set of ports (page 5, paragraph 0065). As to claim 19, Akashi further teaches a substrate (61, fig. 4 and page 4, paragraph 0050) having a first optical waveguide layer (63, fig. 4), a second optical waveguide layer (64, fig. 4) and an optical switching element layer (51, fig. 4).

Regarding claims 2, 21, and 26, Akashi further teaches the array of optical switching elements (51, fig. 9) comprises an array of micro-electro mechanical system (MEMS) devices (page 5, paragraph 0065), each MEMS device having a position controllable reflective surface (page 5, paragraphs 0065, 0069).

Regarding claim 3, Akashi further teaches the array of MEMS devices (51, fig. 9) are grouped in subsets, each subset of MEMS devices being controllable to facilitate transfer of the optical byte of data in parallel from the first set ports to the second set of ports (page 3, paragraph 0033 and page 5, paragraph 0065).

Regarding claims 4 and 27, Akashi further teaches the array of optical switching elements direct the optical byte of data from the first set of ports to the second set of ports using at least one wavelength of the optical byte of data (page 3, paragraph 0038, page 5, paragraph

0065, note that the transmitted and reflected light beams through the switch array 51 each have a wavelength).

Regarding claim 8, Akashi further teaches a control logic for controlling switching of the array of optical switching elements to direct the optical byte of data in parallel from the first set of ports to the second set of ports (page2, paragraph 0012, note that reflecting light elements of the switch array are movable to reflect light from any input port to any output port).

Regarding claim 10, Akashi further teaches the array of optical switching elements directs in parallel the optical byte of data received at the first set of ports to two second sets of ports (page 5, paragraphs 0065, 0067).

5. Claims 1-5, 8, 10, 19, 21-22, and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Kapany (US Patent No: 6,356,679 B1).

Regarding claims 1, 19, and 25, Kapany teaches an optical switch (100, fig. 7), comprising: at least one first set of ports (65a1, 65a2, 65a3, 65a8, fig. 7) for receiving in parallel (col. 6, lines 27-30) an optical byte of data (col. 1, lines 35-38, byte of optical data or information can be transmitted through the optical switch 100); multiple second sets of ports (65b1, 65b2, 65b3, 65b8, and 65c1, 65c2, 65c3, 65c8, fig. 7), each being capable of outputting in parallel the optical byte of data (col. 6, lines 27-35); and an array of optical switching elements (62, fig. 7) disposed between the first set of ports and the multiple second sets of ports (col. 4, lines 61-65, col. 5, lines 3-4, col. 6, lines 27-31), wherein the array of optical switching elements (62, fig. 7) direct the optical byte of data in parallel from the first set of ports to one second set of ports of the multiple second set of ports (col. 6, lines 27-35). As to claim 19, Kapany further

teaches a substrate (60, fig. 5) having a first optical waveguide layer (15a and 65a, 70, 75, fig. 5), a second optical waveguide layer (15b and 65b, fig. 5) and an optical switching element layer (col. 4, lines 48-60 and 60, 62, 63, fig. 5).

Regarding claims 2, 21, and 26, Kapany further teaches the array of optical switching elements (62, fig. 7) comprises an array of micro-electro mechanical system (MEMS) devices (col. 1, lines 25-28, col. 10, lines 43-58), each MEMS device having a position controllable reflective surface (col. 2, lines 38-64, col. 6, lines 21-27).

Regarding claim 3, Kapany further teaches the array of MEMS devices (62, fig. 7) are grouped in subsets, each subset of MEMS devices being controllable to facilitate transfer of the optical byte of data in parallel from the first set ports to the second set of ports (col. 6, lines 6, lines 27-35).

Regarding claim 4, Kapany further teaches the array of optical switching elements (62, fig. 7) direct the optical byte of data from the first set of ports to the second set of ports (col. 7, lines 16-36) using at least one wavelength (for example, $\lambda 1$ in fig. 9) of the optical byte of data.

Regarding claims 5, 22, and 27, Kapany further teaches optical switching elements of the array comprise optical filters (see abstract, col. 2, lines 26-27), each optical filter transferring optical data of a selected wavelength (col. 7, lines 16-36).

Regarding claim 8, Kapany further teaches a control logic for controlling switching of the array of optical switching elements to direct the optical byte of data in parallel from the first set of ports to the second set of port (col. 6, lines 24-26).

Regarding claim 10, Kapany further teaches the array of optical switching elements directs in parallel the optical byte of data received (col. 7, lines 16-36) at the first set of ports (65a, fig. 9) to two second sets of ports (65c1, 65c2, 65b, fig. 9).

6. Claims 11-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Ramadas et al. (US Patent No: 6,836,353 B1).

Regarding claim 11, Ramadas teaches a computing system (300, fig. 3), comprising: at least one computing subsystem having at least one processing unit (319, figs. 3, 4) and at least one bus adapter (323, figs. 3, 4 and 405, fig. 4) through which the processing unit communicates with at least one input/output (I/O) subsystem (Interface, fig. 3); and at least one optical switch (302, figs. 3, 4) optically coupled between the bus adapter and the I/O subsystem (col. 1, lines 5-13, col. 5, lines 17-48), the optical switch (302, figs. 3, 4) transferring in parallel an optical byte of data (col. 2, lines 54-59, col. 5, lines 30-32) received at a first set of ports (313, fig. 3) to at least one second set of ports (309, fig. 3), wherein the one second set of ports being selected (col. 5, lines 25-35) from multiple second sets of ports (309, 311, fig. 3) of the optical switch (302, figs. 3, 4).

Regarding claim 12, Ramadas further teaches control logic for controlling selection of at least one second set of ports to receive the optical byte of data in parallel from the first set of ports (col. 2, lines 49-53, col. 5, lines 33-35, col. 9, lines 58-63).

Regarding claim 13, Ramadas further teaches the optical switch (300, fig. 3) comprises multiple optical switches (302, 304, fig. 3) and the I/O subsystem comprises multiple I/O subsystems (the interface 305, interfaces 311A and 313A, fig. 3), wherein the multiple optical

switches (302, 304, fig. 3) are optically coupled between the bus adapter (Bus 405, system control Bus, fig. 4) and the multiple I/O subsystems (305, 311A, 313A, fig. 3), and the computing system further comprises at least one optical link (optical links or optical fibers that are connected to switching modules 302, 304, in fig. 3) disposed between the bus adapter and a set of ports of each optical switch of the multiple optical switches (col. 5, lines 17-53).

Regarding claim 14, Ramadas further teaches second sets of ports (the ports of optical switches 302 or 304 that are connected to interfaces 313A, 311A, and 305) of at least one optical switch are optically linked to different I/O subsystems (col. 5, lines 48-49).

Regarding claim 15, Ramadas further teaches the switch comprises an array of optical switching elements such as MEMS devices (col. 2, lines 27-33), each MEMS device having a position controllable reflective surface (it is known that MEMS device having a position controllable reflective surface).

Regarding claim 16, Ramadas further teaches the array of optical switching elements directs the optical byte of data from the first set of ports in parallel to the second set of ports using at least one wavelength of the optical byte of data (col. 4, lines 59-67, col. 5, lines 1-5).

7. Claims 1-4, 8-10, 19, 21, and 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Burroughs (US Patent No: 6,925,218 B2).

Regarding claim 1, 19, and 25, Burroughs teaches an optical switch (101, fig. 1A), comprising: at least one first set of ports (102a, fig. 1A) for receiving in parallel an optical byte of data (col. 3, lines 54-67, col. 4, lines 1-2, 25-43, byte of optical data or information can be transmitted through the optical switch 110a); multiple second sets of ports (112b, 112c, fig. 1A),

each being capable of outputting in parallel the optical byte of data (col. 4, lines 28-32, 45-49); and an array of optical switching elements (110a, fig. 1A) disposed between the first set of ports (102a, fig. 1A) and the multiple second sets of ports (112b, 112c, fig. 1A), wherein the array of optical switching elements (110a, fig. 1A) direct the optical byte of data in parallel from the first set of ports to one second set of ports of the multiple second set of ports (col. 4, lines 45-50). As to claim 19, Kapany further teaches a substrate having a first optical waveguide layer, a second optical waveguide layer (col. 3, lines 17-18) and an optical switching element layer (col. 4, lines 32-37, col. 6, lines 55-64 and 600, fig. 6).

Regarding claims 2, 21, and 26, Burroughs further teaches the array of optical switching elements (110a, fig. 1A) comprises an array of micro-electro mechanical system (MEMS) devices, each MEMS device having a position controllable reflective surface (col. 4, lines 56-67, col. 5, lines 1-7).

Regarding claim 3, Burroughs further teaches the array of MEMS devices are grouped in subsets (col. 4, lines 56-57), each subset of MEMS devices being controllable to facilitate transfer of the optical byte of data in parallel from the first set ports to the second set of ports (col. 4, lines 45-49).

Regarding claim 4, Burroughs further teaches the array of optical switching elements (110a, fig. 1A) direct the optical byte of data from the first set of ports (102A, fig. 1A) to the second set of ports (112C, fig. 1A) using at least one wavelength of the optical byte of data (col. 1, lines 30-34, col. 7, lines 30-34).

Regarding claim 8, Burroughs further teaches a control logic for controlling switching of the array of optical switching elements to direct the optical byte of data in parallel from the first set of ports to the second set of port (col. 1, lines 50-53, col. 2, lines 6-21, 55-65).

Regarding claim 9, Burroughs further teaches the first set of ports, the multiple second set of ports, and the array of optical switching elements are bidirectional, allowing optical bytes of data to be transferred in parallel from any one of the first set of ports and the multiple second set of ports to another of the first set of ports and the multiple second sets of ports (col. 4, lines 44-46, col. 6, lines 52-54).

Regarding claim 10, Burroughs further teaches the array of optical switching elements directs in parallel the optical byte of data received at the first set of ports to two second sets of ports (col. 4, lines 40-50).

Regarding claim 24, Burroughs further teaches the first optical layer comprises multiple first sets of ports (col. 2, lines 6-8, col. 4, lines 15-18), and wherein the first optical waveguide layer, the second optical waveguide layer, and the optical switching element layer are each bidirectional (col. 4, lines 44-46, col. 6, lines 52-54).

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramadas et al. (US Patent No: 6,836,353 B1) in view of Kapany (US Patent No: 6,356,679 B1).

Regarding claim 17, Ramadas differs from the claimed invention in that Ramadas does not specifically disclose the MEMS devices of the array of MEMS devices comprise optical filters, each optical filter transferring optical data of a selected wavelength. However, array of MEMS devices with optical filters, wherein each optical filter transfers optical signal of a selected wavelength are well known. For example, Kapany discloses MEMS devices with optical filters (62, fig. 7 and 60, 155a, 155b, fig. 9), wherein each optical filter transfers optical signal of a selected wavelength (col. 2, lines 26-27, col. 7, lines 16-36). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate an array of MEMS with optical filters, as it is taught by Kapany, for the optical switching MEMS array of Ramadas to selectively switch, reflect, or transmit different optical signals.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramadas et al. (US Patent No: 6,836,353 B1) in view of Burroughs (US Patent No: 6,925,218 B2).

Regarding claim 18, Ramadas differs from the claimed invention in that Ramadas does not disclose the first set of ports, the second set of ports, and the array of optical switching elements are bidirectional. Burroughs discloses an optical switching system (101, fig. 1A) having input and output receiving modules (112a, 112b, 112c, fig. 1A) with an optical switching array (110a, fig. 1A) that are bidirectional (col. 4, lines 44-46, col. 6, lines 52-54). It would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a bidirectional optical switch array such as the one of Burroughs for the optical switch array of Ramadas to provide bidirectional transmission and switching between different input ports and output ports.

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kapany (US Patent No: 6,356,679 B1) in view of Ishii et al. (US Patent No: 6,912,336 B2).

Regarding claim 20, Kapany differs from the claimed invention in that Kapany does not disclose an optical vias disposed within some layers of the multiple layers for facilitating passing of the optical byte of data between the first optical waveguide layer, the optical switching layer, and the second optical waveguide layer. Ishii discloses a method of manufacturing an optical switch device (fig. 2, 3A), wherein vias are formed in an interlayer of a dielectric layer (col. 8, lines 1-8). As it is taught by Ishii, it would have been obvious to a person of ordinary skill in the art at the time of invention to provide optical vias in the layers of optical input or output waveguides or in the switching layer of Kapany to further facilitate the transmission of light signals.

12. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kapany (US Patent No: 6,356,679 B1) in view of Huang et al. (US Patent No: 6,614,954 B2).

Regarding claim 23, Kapany differs from the claimed invention in that Kapany does not disclose the device is integrated within a multichip module containing at least one processing unit. Incorporating optical switching devices within multichip modules with processing units are well known. For example, Huang teaches a multichip module (20, fig. 3) with processing units (DSPs, fig. 3) and optical switching arrays (18, 26, fig. 3 and col. 9, lines 24-36). As it is taught by Huang, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the optical switching array of Kapany in a multichip module having a

processing unit, to provide control for the switch and to selectively transmit or switch different light signals.

13. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. R. Sedighian whose telephone number is (571) 272-3034. The examiner can normally be reached on 9 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M. R. Sedighian

M. R. SEDIGHIAN
PRIMARY EXAMINER